MMIC Power Amplifier Adaptively Linearized With RF Coupled Active Bias Circuit For W-CDMA Mobile Terminals Applications

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Abstract — **A new on-chip linearizer self-adapting to the input power has been devised and implemented to a high linear monolithic microwave integrated circuit (MMIC) power amplifier for 1.95 GHz wide-band code division multiple-access (W-CDMA) system. The linearizer consists of InGaP/GaAs heterojunction bipolar transistor (HBT) active bias circuit and reverse biased junction diode of which dynamic admittance to input power level varies adaptively to control RF transmission power to bias circuit. The proposed linearizer effectively improves the gain compression with little insertion power loss, and more importantly, it consumes no additional die area and DC power. The HBT MMIC power amplifier with the integrated linearizer exhibits a maximum output power of 30.3 dBm, a power gain of 27.5 dB, a power added efficiency of 42 % at the maximum output power under an operation voltage of 3.4 V, and adjacent channel leakage power ratio of –38dBc at 27 dBm of output power.**

I. Introduction

Third generation handset system such as Wide-Band Code Division Multiple-Access (W-CDMA) employs a wider frequency spectrum for higher data transmission, and uses the linear modulation scheme. Handsets based on W-CDMA system demand a lower adjacent channel leakage power ratio (ACLR) performance for power amplifier in order to minimize spectral regrowth and maintain modulation accuracy. To realize high linearity for W-CDMA portable application, it is essential to improve the gain compression point resulting in AM-AM distortion. To meet low cost and small chip size requirement as well for handset applications, several reports on HBT MMIC power amplifier equipped with on-chip linearizer have been introduced [1-5]. The gain compensation was achieved with predistortion of RF input signal prior to amplification [1] or with integrated bias circuit maintaining the amplifier bias unchanged [2-5]. Even though the latter is more adequate to be integrated into an MMIC without any significant DC power consumption and additional chip area, if not controlled properly, there are some possible risks to have either excessive RF power loss to the bias circuit at low output power level or insufficient gain compensation around the gain compression point.

In this paper, we demonstrate a new on-chip active bias circuit linearizer compensating the gain compression adaptively to the input power level in order to obtain effective gain compensation and minimize power loss through the linearizer. The proposed linearizer is composed of active bias circuit shunted to RF input through a reverse biased diode, and utilizing the dynamic admittance of the diode to the input power. This technique requires no additional DC current, has little insertion loss, and effectively improves the linearity of the amplifier.

II. Adaptive Linearization Technique Using A Reverse Biased Diode

Design of base bias circuit of a HBT MMIC power amplifier is one of the key tasks to obtain high linear output power for handset application due to the significant change of base bias point according to the input power. When the large RF voltage and current signal are applied across the base-emitter junction of HBT amplifier, junction diode bias point decreases due to increase of the rectified average DC current of base-emitter diode. Therefore, the decrease of base-emitter voltage, V_{BE}, of the HBT amplifier results in the decrease of transconductance, causing gain compression of the amplifier.

To improve the gain compression, we devise an on-chip linearizer which controls the V_{BE2} of bias HBT compensating the amplifier V_{BE1} drop by partial coupling RF power through coupling component as shown in Fig.1. Since the insertion power through the coupling component is determined by the transmission coefficient, S_{21}, and input power, as input power increases, V_{BE1} of HBT_1 is more effectively compensated resulting in improvement of P_1dB of the power amplifier. However, large S_{21} value of coupling component has a risk to increase the insertion power loss significantly through coupling component

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even at small output power level below the compression point as shown in Fig.2. In order to have more linearization for higher P_1dB over 30dBm and small power loss less than –40dBm through the bias circuit at low output power level, an adaptable coupling with S_{21} value increasing with the input power is needed between the input port of the amplifier and the base node of the bias HBT_2.

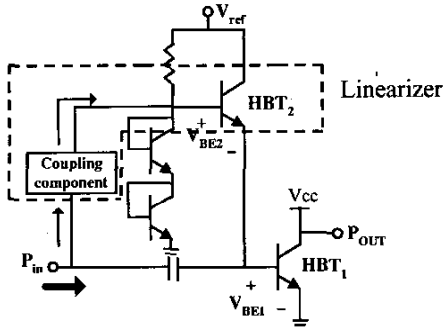

Fig.1 Schematic diagram of the linearizer with active bias circuit shunted to RF input path through coupling component.

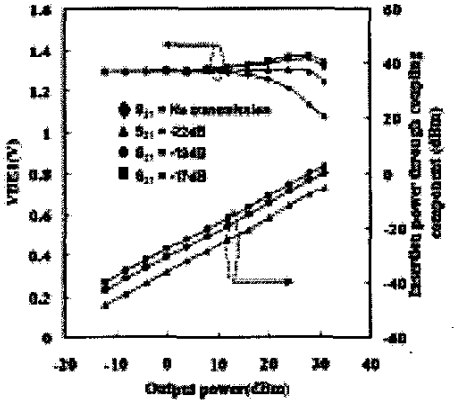

Fig.2 Compensation effect on V_{BE1} of HBT_1 for different value of S_{21} of coupling component.

To obtain a small S_{21} at smaller input power and an appropriately increased S_{21} value at higher output power, a linearizer is designed in this work with a reverse biased emitter-base junction diode as the coupling component. Fig.3 shows the simplified equivalent circuit of the reverse biased diode that is implemented with base emitter junction of the HBT. It is composed of a variable capacitance and a conductance that are dependent on input power level. The S_{21} of the reverse biased junction diode is derived as follows from the equivalent circuit as a function of source and load impedance, Z_1 and Z_2:

$$S_{p21}=\frac{\sqrt{R_1}}{\sqrt{R_2}}\cdot\frac{Z_2+Z_2^*}{\dfrac{R_d}{1+j\omega C_d R_d}+Z_1+Z_2} \quad (1)$$

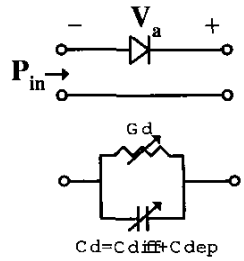

Fig.3 Equivalent circuit of the reverse biased diode.

Even though the junction diode is reverse biased by DC voltage, V_a, the reverse biased diode reaches forward biased condition for duration of large positive RF signal swing. It is expected that the equivalent capacitance C_d increases by adding the forward diffusion capacitance, C_{diff}, and also the equivalent conductance of reverse biased diode increases. Fig.4 shows the measured variation of capacitance and resistance of the reverse biased diode extracted from the equivalent circuit as a function of RF input power at 1.95GHz. The capacitance of reverse biased diode increases by 0.1pF compared to the capacitance at –20dBm of input power, and the resistance drastically decreases by about a factor of six as RF input power increases as much as 20dBm.

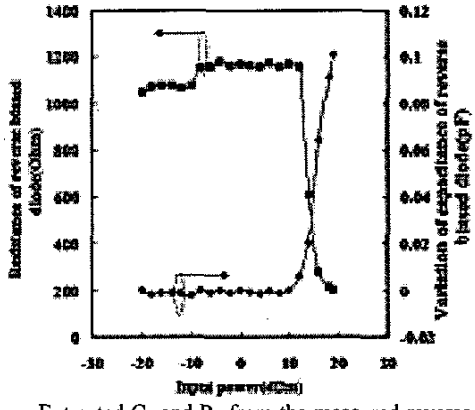

Fig.4 Extracted C_d and R_d from the measured reverse biased diode.

The dynamic S_{21} of the reverse biased diode caused by the variation of C_d and R_d with the input power is evaluated by using the equation (1), and is described in Fig.5. The S_{21} of reverse biased diode exhibits constant value at -30~-20dBm of small input power level, and slightly decreases due to decrease of impedance seen to base of power stage HBT at -20~10dBm of medium input power level. When input power reaches near 20dBm, the S_{21} of the reverse biased diode drastically increases due to

change of C_d and R_d as shown in Fig.4. The S_{21} is determined by varying the diode junction area for adaptable bias control function to the input power.

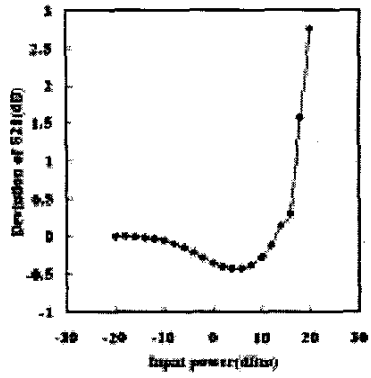

Fig.5 The calculated deviation of S_{21} for reverse biased diode.

Fig.6 illustrates the circuit topology of new adaptive linearizer composed of an active bias circuit shunted to RF input path through the optimized reverse biased diode. The linearizer operates according to the following mechanism.

1) The reverse biased diode makes partial RF signal path to base node of the bias HBT, HBT_4.
2) As input power increases, the power delivered to the base node of HBT_4 increases, and the large injected RF signal swing is also applied across base-emitter diode of HBT_4 as well as HBT_3. The clipped average DC current increases, and the clipped average junction voltage of HBT_4 decreases. The decrease of V_{BE4} compensates the decrease of base-emitter junction voltage of the amplifier HBT, HBT_3 (V_{BE3}).
3) When input power reaches up to 20dBm, S_{21} of reverse biased diode increases resulting in coupling of more input power to the base of HBT_4. The increase of transmission power makes V_{BE4} more drastically decrease, therefore the decrease of V_{BE3} is effectively compensated even around the compression point.

Since the emitter area of the bias HBT_4 is much smaller than that of the amplifier HBT_3, the impedance seen to the base node of HBT_4 is very large compared to that of HBT_3, so the most of RF input signal goes through to HBT_3. Therefore, the amounts of the inserted RF signal to the base of HBT_4 dose not affect both of small and large signal gain even if there is more insertion RF power through the bias HBT_4. Fig.7 describes the calculated gain compression and insertion power through the bias HBT_4 for the different emitter area (S_E) of reverse biased diode. In case of S_E=120μm^2, inserted signal power through the bias HBT_4 is calculated as small as 0.3dBm at 20dBm of input power which is maximum output power value of the first stage amplifier. We have optimized the emitter size of reverse biased diode to 120 um^2 that has a capacitance value of 0.81 pF similar to the optimized coupling capacitor [5] and a resistance value of 875 Ohm. This admittance value does not affect the gain loss but introduce higher linearity improvement even in high RF output power level.

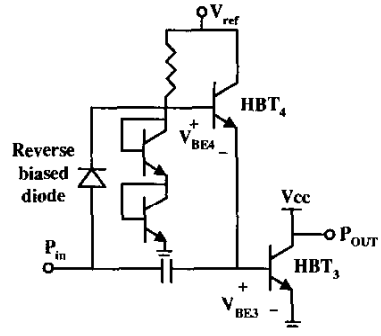

Fig.6 Schematic diagram of the linearizer with active bias circuit shunted to RF input path through a reverse biased diode.

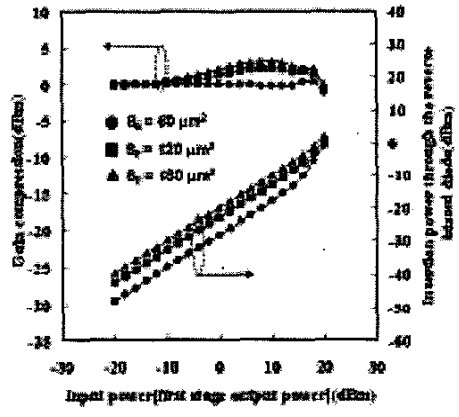

Fig.7 The calculated gain compression and insertion power through bias HBT_4 for the different emitter area (S_E) of reverse biased diode.

III. Circuit Design And Chip Implementation

A two-stage HBT MMIC power amplifier including an active bias circuit with the adaptive on-chip linearizer, input matching network and inter-stage matching network was designed and fabricated using an InGaP/GaAs HBT technology. Fig.8 illustrates the photograph of the

fabricated MMIC chip. Total chip size is as small as 0.87mm×1.00mm. The InGaP/GaAs HBTs are comprised of units with 60 μm^2 emitter area. The 12-unit multiple HBT cells (S_E=720 μm^2) are utilized in the drive stage and the 48-unit multiple HBT cells (S_E=2880 μm^2) are utilized in the power stage.

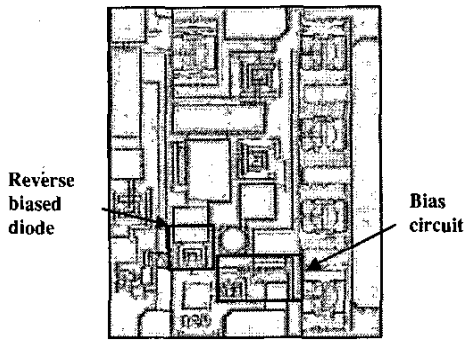

Fig.8 Photograph of the power amplifier for W-CDMA mobile terminals.

IV. Measured Performance

Fig.9 shows the gain compression and ACLR as a function of output power for the MMIC power amplifiers devised with the adaptable linearizer compared to that with typical linearizer using MIM capacitors of 0.4pF and 0.8pF and thus having constant S_{21} value as shown Fig.2. MIM capacitor of 0.4pF exhibits –22dB of S_{21} value, and 0.8pF does –17dB. ACLR measurement is achieved using 3.84 Mcps W-CDMA modulated signal in 5 MHz offset frequency band. The gain compression point of the amplifier with reverse biased diode is increased as much as 1.7dB compared to that with capacitor of 0.8pF [5], and 4dB compared to that with capacitor of 0.4pF. ACLR of the amplifier with reverse biased diode is improved over 7.5dBc at an output power of 27dBm compared to that with capacitor of 0.8pF and 0.4pF. This improvement confirms that the adaptive linearizer using reverse biased diode is effective for high linearity. The MMIC power amplifier exhibits a maximum output power of 30.3 dBm along with power added efficiency as high as 42 %.

V. Conclusion

A new adaptive linearization technique that utilizes an active bias circuit shunted to RF input path through a reverse biased diode is described, and it was explicitly demonstrated that the new adaptive linearization technique was very effective increasing the gain compression point at high output power level. This technique requires no additional DC current, no additional die area, and has little insertion loss. The high linear two-stage HBT MMIC power amplifier with the on chip adaptive linearizer has the power gain of 27.5 dB, the maximum output power of 30.3 dBm, 42 % of the power added efficiency at output power of 30.3 dBm. ACLR is observed – 38dBc at output power of 27 dBm that confirm all of W-CDMA specifications.

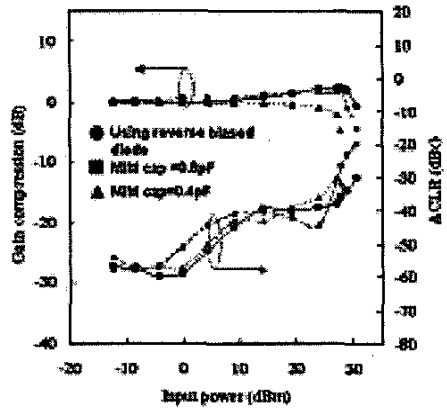

Fig.9 Gain compression and ACLR of the amplifier with reverse biased diode and the amplifier with linearizer that utilized MIM capacitor (0.4pF: simulation, 0.8pF: measurement).

Acknowledgement

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